# Bi-weekly Status Report 5 Senior Design, December 2020, Team 14

Introduction of Real-World Signals and Systems into ECpE DSP Laboratory Curriculum

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#### **Progress Summary:**

Over the past four weeks we have finished the filter lab document and generated the necessary audio files for filtering and sampling in Matlab. We also continued hardware development with physical builds of the validation PMods. We obtained familiarity with applicable design tools, and worked on the user software side of the project. We also completed our third lightning talk and developed a contingency plan for the Coronavirus pandemic.

#### Individual Contributions by Team Member:

- Brady Anderson (Biweekly: 25; Cumulative: 74)
  - Drafted a second revision of the Design Document
  - Designed and began implementing a COVID-19 Contingency Plan
  - Completed Lightning Talk 3
  - Completed PWM IP core development
  - Began testing implementation methods for parallelism between PWM signal route and primary firmware
  - Began reading FreeRTOS development documentation
- Sam Burnett (Bi-weekly: 10.5, Cumulative: 71)
  - Assembled DAC and ADC PMod Boards for testing
  - Generated audio files for the filter lab
  - Assisted with the filter lab document
  - Completed Lightning Talk 3
  - Drafted a COVID-19 Contingency Plan
- Mitchell Hoppe (Weekly: 12; Cumulative: 62.0)
  - Finished back-end of the GUI
  - Continued work on CLI front-end
  - Researched creating GUI's in Matlab
- Max Kiley (Biweekly: 20; Cumulative: 66)
  - Drafted a second revision of the Design Document
  - Designed and began implementing a COVID-19 Contigency Plan
  - Completed Lightning Talk 3.
  - Finished working on Noise Reduction Lab
  - Reviewed Fourier Series and other EE 224 concepts.
- Emily Lagrant (Biweekly: 14; Cumulative: 65)
  - Finished first draft of noise reduction lab
  - Edited and revised noise reduction lab

- Revised noise reduction lab for online classes
- Tested noise reduction lab
- Sent the noise reduction lab to Dr. Dickerson for EE 224
- o Made contingency plan and had several meetings to plan around the pandemic
- Continued research for more labs
- Isaac Rex (Bi-Weekly:  $\frac{d}{dt}[.5t^4 + 3t^3 + 12t^2 + 10t + 5]$ , t = -3; Cumulative: 74.5)
  - Reviewed and edited noise reduction lab
  - o Finished Rev 2 of Design Doc
  - Designed and began implementing a COVID-19 Contingency Plan
  - Finished Lightning Talk 3
  - Obtained necessary hardware to continue testing and developing labs
  - Assessment of EE 224 lab progress and goals for EE 324

## Pending Issues:

• There are currently no pending issues

### Plans:

- Isaac:
  - Complete final draft of CyDAQ introduction lab
  - Create solution manual for CyDAQ introduction lab
  - Continue working on speaker board for CyDAQ
  - Continue working on final project lab manuals
- Emily:
  - Receive feedback for noise reduction lab
  - Create noise reduction lab for CyDAQ (not online lab) use
  - Begin work on further labs
- Brady:
  - Continue considering FreeRTOS implementation strategies
  - Test Sam's PWM intuition lab with prototype PMOD
  - Integrate PWM IP core with XADC firmware
- Sam:
  - Develop a remote testing and evaluation plan for the PMods
  - Implement the pending changes in the board files
  - Assist with further lab development file generation requirements
- Max
  - Continue work to help implement CyDAQ labs
  - Continue to work on Final Project lab.
- Mitch
  - Finish CLI so that it is ready for development use.
  - Begin work on creating and integrating the Matlab GUI with the existing python code